Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**A1**

**A0**

**D0**

**D1**

**D2**

**VSSO**

**VSSO**

**VSS**

**VSS**

**D3**

**D4**

**D5**

**D6**

**D7**

**CE**

**A4**

**A5**

**A6**

**A7**

**A12**

**N/C**

**VCC**

**VCCO**

**WE**

**N/C**

**A8**

**A9**

**A11**

**A2 A3**

**A10 OE**

**.136”**

**.101”**

**NOTE: Recommend bonding to at least 1 each VSS and VSSO pin**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Geometry: 19803**

**APPROVED BY: DK DIE SIZE .101” X .136” DATE: 9/23/21**

**MFG: ATMEL THICKNESS .020” P/N: AT28C64B**

**DG 10.1.2**

#### Rev B, 7/1